	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	6297104.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:43
2	BRS	L2	5	5840602.pn. or 6150243.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:46
3	BRS	L3	2984	(logic adj1 device) and (memory adj1 device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:47
4	BRS	L4	44	(first adj1 transistor) near10 (dielectric adj1 layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:55
5	BRS	L5	4	3 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:51

	Type	L #	Hits	Search Text	DBs	Time Stamp
[illegible]	[illegible]	[illegible]	49	(first adj1 transistor) near15 (dielectric adj1 layer)	USPAT; US-PGP UB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 21:56
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	USPAT; US-PGP UB; EPO; JPO; DERWENT; IBM_TDB	[illegible] 21:56
[illegible]	BRS	L8	3163	(transistor) near15 (dielectric adj1 layer)	USPAT; US-PGP UB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 22:36
[illegible]	BRS	L9	79	3 and 8	USPAT; US-PGP UB; EPO; JPO; DERWENT; IBM_TDB	[illegible] 21:57
[illegible]	BRS	L10	69	9 and thickness	USPAT; US-PGP UB; EPO; JPO; DERWENT; IBM_TDB	[illegible]

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	37	10 and channel adj1 region	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/[illegible] 21:[illegible]
12	BRS	L12	13	11 and oxidation	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/[illegible] 21:59
13	BRS	L13	31	11 and oxid$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/[illegible] 22:15
14	BRS	L14	5066	(transistor) near15 (dielectric adj1 layer or silicon adj1 dioxide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 22:46
15	BRS	L15	[illegible]	[illegible] and L14	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/[illegible] 22:46

	Type	L #	Hits	Search Text	DBs	Time Stamp
[illegible]	BRS	[illegible]	100	15 and channel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/[illegible] [illegible]:47
[illegible]	BRS	L17	69	16 and (source and drain)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:17
[illegible]	BRS	[illegible]	47	3 and gate near1 oxide$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:18
19	BRS	L19	389	18 and transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:18
[illegible]	BRS	L20	344	19 and thickness	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:18

	Type	L #	Hits	Search Text	DBs	Time Stamp
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
21	BRS	L21	288	20 and channel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:18
22	BRS	L22	258	21 and (source and drain)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:18
23	BRS	L23	129	22 and oxidation	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:19
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
25	BRS	L25	13	23 and second adj1 transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/03/28 23:20

	U	1	Document ID	Title	Current OR
[illegible]	☐	☐	US [illegible] A1	Structure and method for dual gate oxide thicknesses	438/275
[illegible]	☐	☐	US 20020004276 A1	Structure and method for dual gate oxide thicknesses	438/275
[illegible]	☐	☐	US [illegible] B1	Method of manufacturing semiconductor device in which hot carrier resistance can be improved and silicide layer can be formed with high reliability	[illegible]
[illegible]	☐	☐	US [illegible] B1	Structure and method for dual gate oxide thicknesses	438/275
5	☐	☐	US 6232631 B1	Floating gate memory cell structure with programming mechanism outside the read path	257/315
6	☐	☐	US 6048760 A	Method of forming a self-aligned refractory metal silicide contact using doped field oxide regions	438/225
7	☐	☐	US 5949706 A	Static random access memory cell having a thin film transistor (TFT) pass gate connection to a bit line	365/156
[illegible]	☐	☐	US [illegible] A	Memory cell having a plural transistor transmission gate and method of formation	365/189.03
9	☐	☐	US 5777347 A	Vertical CMOS digital multi-valued restoring logic device	257/24
10	☐	☐	US 5257095 A	Common geometry high voltage tolerant long channel and high speed short channel field effect transistors	257/315
11	☐	☐	US 5045489 A	Method of making a high-speed 2-transistor cell for programmable/EEPROM devices with separate read and write transistors	438/258
12	☐	☐	US 4931411 A	Integrated circuit process with TiN-gate transistor	438/291

	U	1	Document ID	Title	Current OR
1	☐	☐	US 4814854 A	Integrated circuit device and process with tin-gate transistor	257/382